



AGIGARAM[®]

DDR4 Registered Non-Volatile DIMM (NVDIMM-N)

AGIGA8811 (“Komodo1”) Advance Datasheet

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Revision History

| Date | Description of Changes | Document No. Revision |
|-----------|---|-----------------------|
| Dec 2019 | Initial Release | 00 |
| June 2020 | Added support for DDR-3200 | 01 |
| Aug 2020 | Changed to IFX Logo and company name Minor edits to Product Overview section Changed reference from “Backup” to “Save” to be consistent with JEDEC standard Updated Figure 2 to show SAVE_n pin (230) connects to AGIGA Data Mover instead of AGIGA Controller Updated t_{RC} parameter for PC4-3200 Added Timing Parameters and Operating Conditions to include 32GB module values Added “12V” parameter to Operating Conditions Updated I_{DDx} values and added 32GB values Updated J_{BACKUP}/J_{SAVE} values for both 16GB and 32GB Clarified Operating Conditions were measured using a 3200 speed module Updated DDR4 IDDx Specification and Conditions table Updated LED section to indicate a single multi-color 3 in 1 LED is used | 02 |

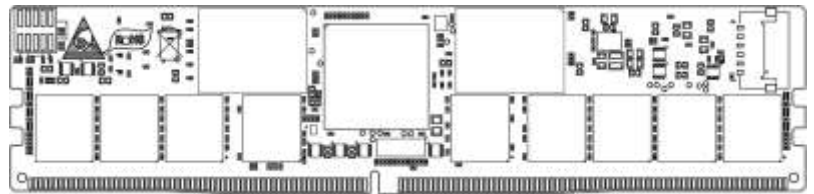
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AGIGARAM® DDR4 Registered NVDIMM-N

AGIGA8811-016xyz 16GB (SRx4)

AGIGA8811-032xyz 32GB (SRx4)



Module height: 31.25mm (1.23in)

Figure 1: 288-Pin Registered NVDIMM-N

1 Product Overview

The AGIGARAM® Non-Volatile DIMM (NVDIMM) is a new class of non-volatile memory developed to meet the need for higher-density, higher-performance memory for enterprise-class storage and server applications. By combining DRAM, Flash, an intelligent system controller and an ultracapacitor power source, AGIGARAM provides a highly reliable memory subsystem that runs with the latency and endurance of the fastest DRAM, and with the persistence of Flash. Previously, designers have used batteries to maintain their data during power outages. Others have moved toward new flash-based or emerging non-volatile technologies for memory persistence, but these options falls short of DRAM in terms of latency, speed, endurance and reliability. AGIGARAM enables the fastest possible system performance while also eliminating the many headaches associated with batteries, such as hazardous material disposal, short operating life and periodic maintenance.

The AGIGARAM DDR4 NVDIMM is designed to comply with the JEDEC-defined NVDMM-N type. It is intended to operate with standard server platforms that have implemented the ADR (Asynchronous DRAM Re-Fresh) feature, although it is possible to integrate into systems that do not have this feature (please contact Agiga for assistance).

During normal operation, the AGIGARAM DDR4 NVDIMM appears as a standard JEDEC-compliant registered DDR4 DIMM to the host system, providing all the benefits and speed of a high-speed, high-density SDRAM. In the event of a power loss, the AGIGARAM controller takes control of the SDRAM, transferring its contents to flash memory using energy from a battery-free power source, thereby preserving all the SDRAM data. After power is restored, the host system sends a RESTORE command to the AGIGARAM controller to transfer the contents in the flash back into the SDRAM and returns control to the host system.

Below are a few of the use cases that can take advantage of the features of an NVDIMM:

- Storage Arrays: Non-volatile write cache, storage tiering, SSD wear-out protection
- Big Data: Fast IOPS workloads, in-memory database, log acceleration
- Virtualization: VM consolidation
- Cloud Computing/AI/IoT: Byte-level transaction processing, metadata store, low-latency look-up

2 System Block Diagram

The AGIGARAM NVDIMM is available as a JEDEC standard 288-pin DDR4Registered DIMM, with a 72-bit wide data bus. The Figure below shows the system-level block diagram.

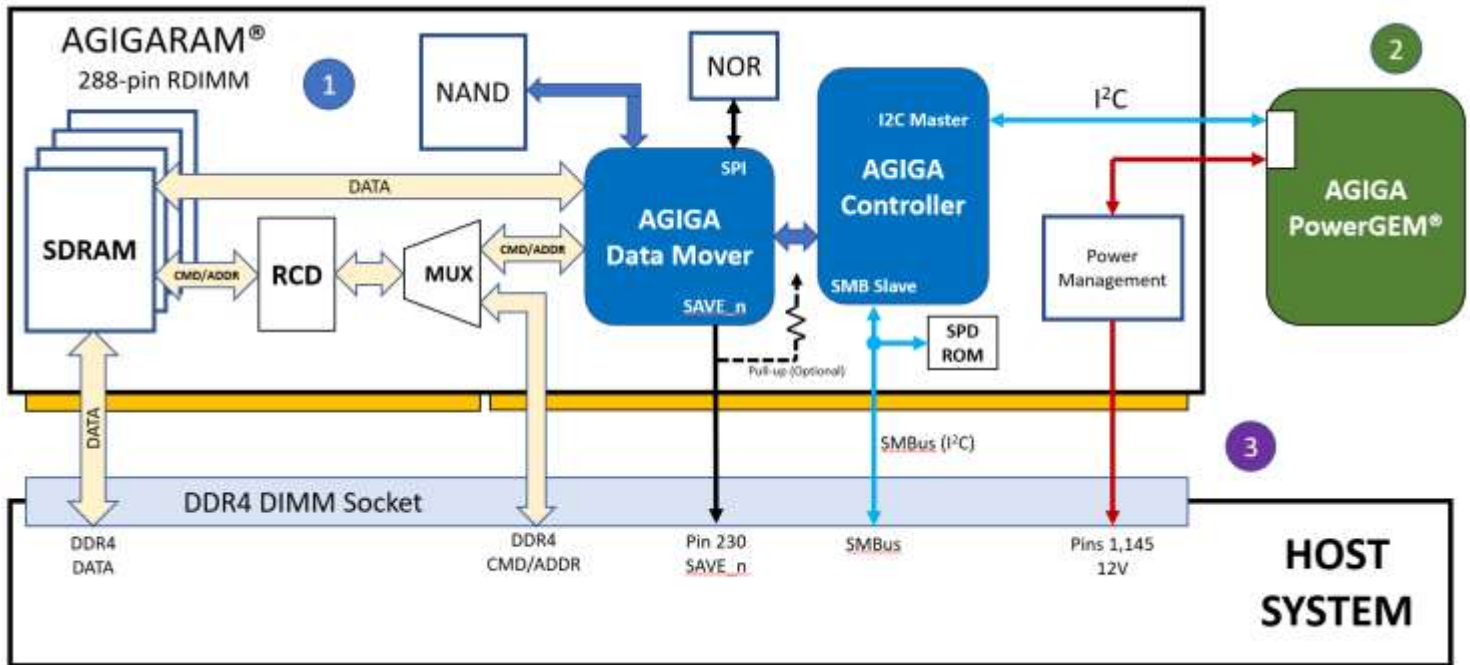


Figure 2: AGIGARAM DDR4NVDIMM System Block Diagram

As this Figure shows, the AGIGARAM System is comprised of two separate modules connected by a cable:

- 1 **AGIGARAM NVDIMM**— standard RDIMM pin-out module contains all of the DDR4 memory components, NAND Flash, power management and ancillary components, as well as the AGIGARAM controller that manages data transfer and host coordination. The interface to the host complies with the JEDEC DDR4 DIMM interface standard.
- 2 **PowerGEM® (Green Energy Module)** — provides power to the AGIGARAM NVDIMM during a Save. This ultracapacitor based power supply is charged during runtime via the 12V supplied through the NVDIMM or from 12V directly connected to the module if available. At power interruption, the PowerGEM ensures continuity of power while the SDRAM contents are saved to the NAND flash. When the SAVE_n operation completes, the AGIGARAM NVDIMM shuts down completely without requiring back-up power. In contrast, a battery-backed DIMM may lose its contents after a period of time depending on how much energy is available.
- 3 **Host Managed Energy Source (Optional)** — The AGIGARAM DDR4 NVDIMM can support host provided Save power through the DIMM socket interface pins 1 and 145. The acceptable voltage range is between from 12V down to 4V. See the electrical specifications table for specific NVDIMM Save energy requirements.

3 Key Features

- DDR4 Non-Volatile DIMM (NVDIMM)
 - NVDIMM-N type per JEDEC definition
 - Highly reliable persistent memory solution
 - No wear or endurance issues
 - DRAM, Flash, Controller and Power Management integrated in a single module
 - 16 GB and 32 GB density supported (please inquire if other densities are desired)
 - AES-256 Encryption
 - DRAM with integrated analog mux feature eliminates the need for external muxes in the DRAM data path providing superior rank margin performance vs other solutions
 - Standard JEDEC Registered Dual Inline Memory Module (RDIMM) 288-pin connector
 - DDR4 functionality and operations supported
 - Fast data transfer rate: up to PC4-3200
 - Single-rank x4 design
 - Supports SDRAM ECC error detection and correction by host memory controller
 - Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
 - On-board I²C/SMB temperature sensor with integrated serial presence-detect (SPD) EEPROM
 - 16 internal device banks
 - Timing – cycle time
 - 0.625ns @ CAS Latency = 22 (DDR4-3200)
 - 0.682ns @ CAS Latency = 21 (DDR4-2933)
 - 0.750ns @ CAS Latency = 19 (DDR4-2666)
 - 0.833ns @ CAS Latency = 17 (DDR4-2400)
 - Can be powered by external PowerGEM or through central power (over 12V rail) during Save
 - 31.25mm DIMM height
- PowerGEM Ultracapacitor Module (see separate datasheet for specifications)
 - Highly reliable, battery-free power source
 - Powers the AGIGARAM NVDIMM when the system host loses power
 - 12V charging over DIMM interface (or external connection if available)
 - 5-year operating life (typical, can be tailored to user system requirements)
 - Safe and “green”
 - Low Total Cost of Ownership (TCO), no maintenance required over the product life
 - RoHS, REACH and UL/cUL/CB/CE compliant, no hazardous material issues
- System-Level Features
 - In-system health monitoring
 - Automatic history tracking: tracks critical internal system parameters
 - Online firmware upgrade support
 - Supports JEDEC Byte Addressable Energy Backed Interface (BAEBI) Specification
 - Supports AgigA Vendor Page Specification for additional features

4 Host Coordination Using AGIGARAM Control Signal

The AGIGARAM module will conform to the JEDEC defined NVDIMM-N type specification.

An NVDIMM requires coordination between the host and memory. For example, the host must take steps to ensure that a memory write operation is not in progress when power suddenly fails to prevent memory contents from becoming corrupted.

For safe operation, AGIGARAM requires that the host meets the following requirements:

- The host must have early warning that power is failing, allowing it to perform an orderly shutdown.
- The host must put memory into a safe state before handing it off to the AGIGARAM subsystem. The safe SDRAM state is its Self-Refresh mode. Once this state is entered, the Clock Enable (**CKE0**) signal is low and all SDRAM control signals except **CKE0** and **RESET#** are “don’t care.” The SDRAM refreshes itself in this mode, preserving its contents as the host-to-AGIGARAM switch (and back) is made.
- When the host regains control of the DDR4 SDRAM from the AGIGARAM controller (for example after performing a **SAVE_n** or **RESTORE** operation), the host must remove the DDR4 SDRAM from Self-Refresh. The host should take care not to assert the **RESET#** signal after a **RESTORE** operation completes, as the **RESET#** signal resets the internal SDRAM state machine and the restored data can be potentially lost.

Table 1: Key Timing Parameters

| Industry Nomenclature | Data Rate (MT/s) | | | | t _{RCD} (ns) | t _{RP} (ns) | t _{RAS} (ns) | t _{RC} (ns) | CL-t _{RCD} -t _{RP} |
|-----------------------|------------------|---------|---------|---------|--------------------------|-------------------------|--------------------------|-------------------------|--------------------------------------|
| | CL =22 | CL = 21 | CL = 19 | CL = 17 | | | | | |
| PC4-3200 | 3200 | 2933 | 2666 | 2400 | 13.75 | 13.75 | 32 | 45.75 | 22-22-22 |
| PC4-2933 | | 2933 | 2666 | 2400 | 14.32 | 14.32 | 32 | 46.32 | 21-21-21 |
| PC4-2666 | | | 2666 | 2400 | 14.25 | 14.25 | 32 | 46.25 | 19-19-19 |
| PC4-2400 | | | | 2400 | 14.16 | 14.16 | 32 | 46.16 | 17-17-17 |

Table 2: Addressing

| Parameter | 16GB | 32GB |
|-------------------------------|-----------|-----------|
| Row address | A[16:0] | A[17:0] |
| Column address | A[9:0] | A[9:0] |
| Device bank group address | 4 BG[1:0] | 4 BG[1:0] |
| Device bank address per group | 4 BA[1:0] | 4 BA[1:0] |
| Module rank address | CS0_n | CS0_n |
| Page size | 512B | 512B |

Table 3: Part Numbers and Timing Parameters

| Part Number(s) | Module Density | Configuration | Memory Clock/ Data Rate | Clock Cycles (CL-t _{RCD} -t _{RP}) |
|----------------|----------------|---------------|-------------------------|--|
| AGIGA8811-016 | 16GB | 2 Gig x 72 | 0.625ns/3200 MT/s | 22-22-22 |
| AGIGA8811-032 | 32GB | 4 Gig x 72 | 0.625ns/3200 MT/s | 22-22-22 |

5 Pin Assignments and Descriptions

Table 4: NVDIMM Pin Assignments

| Front Side Pin Label | Pin | Pin | Back Side Pin Label | Front Side Pin Label | Pin | Pin | Back Side Pin Label |
|-------------------------------------|-----|-----|---------------------|-------------------------------------|-----|-----|---------------------|
| 12V | 1 | 145 | 12V | VSS | 39 | 183 | DQ25 |
| VSS | 2 | 146 | VREFCA | TDQS12_t, DQS12_t, DM3_n, DBI3_n | 40 | 184 | VSS |
| DQ4 | 3 | 147 | VSS | TDQS12_c, DQS12_c, NC | 41 | 185 | DQS3_c |
| VSS | 4 | 148 | DQ5 | VSS | 42 | 186 | DQS3_t |
| DQ0 | 5 | 149 | VSS | DQ30 | 43 | 187 | VSS |
| VSS | 6 | 150 | DQ1 | VSS | 44 | 188 | DQ31 |
| TDQS9_t, DQS9_t, DM0_n, DBI0_n | 7 | 151 | VSS | DQ26 | 45 | 189 | VSS |
| TDQS9_c, DQS9_c, NC | 8 | 152 | DQS0_c | VSS | 46 | 190 | DQ27 |
| VSS | 9 | 153 | DQS0_t | CB4,NC | 47 | 191 | VSS |
| DQ6 | 10 | 154 | VSS | VSS | 48 | 192 | CB5,NC |
| VSS | 11 | 155 | DQ7 | CB0,NC | 49 | 193 | VSS |
| DQ2 | 12 | 156 | VSS | VSS | 50 | 194 | CB1,NC |
| VSS | 13 | 157 | DQ3 | TDQS17_t, DQS17_t, DM8_n, DBI8_n | 51 | 195 | VSS |
| DQ12 | 14 | 158 | VSS | TDQS17_c, DQS17_c, NC | 52 | 196 | DQS8_c |
| VSS | 15 | 159 | DQ13 | VSS | 53 | 197 | DQS8_t |
| DQ8 | 16 | 160 | VSS | CB6,NC | 54 | 198 | VSS |
| VSS | 17 | 161 | DQ9 | VSS | 55 | 199 | CB7,NC |
| TDQS10_t, DQS10_t, DM1_n, DBI1_n | 18 | 162 | VSS | CB2,NC | 56 | 200 | VSS |
| TDQS10_c, DQS10_c, NC | 19 | 163 | DQS1_c | VSS | 57 | 201 | CB3,NC |
| VSS | 20 | 164 | DQS1_t | RESET_n | 58 | 202 | VSS |
| DQ14 | 21 | 165 | VSS | VDD | 59 | 203 | CKE1,NC |
| VSS | 22 | 166 | DQ15 | CKE0 | 60 | 204 | VDD |
| DQ10 | 23 | 167 | VSS | VDD | 61 | 205 | RFU |
| VSS | 24 | 168 | DQ11 | ACT_n | 62 | 206 | VDD |
| DQ20 | 25 | 169 | VSS | BG0 | 63 | 207 | BG1 |
| VSS | 26 | 170 | DQ21 | VDD | 64 | 208 | ALERT_n |
| DQ16 | 27 | 171 | VSS | A12/BC_n | 65 | 209 | VDD |
| VSS | 28 | 172 | DQ17 | A9 | 66 | 210 | A11 |
| TDQS11_t, DQS11_t, DM2_n, DBI2_n | 29 | 173 | VSS | VDD | 67 | 211 | A7 |
| TDQS11_c, DQS11_c, NC | 30 | 174 | DQS2_c | A8 | 68 | 212 | VDD |
| VSS | 31 | 175 | DQS2_t | A6 | 69 | 213 | A5 |
| DQ22 | 32 | 176 | VSS | VDD | 70 | 214 | A4 |
| VSS | 33 | 177 | DQ23 | A3 | 71 | 215 | VDD |
| DQ18 | 34 | 178 | VSS | A1 | 72 | 216 | A2 |
| VSS | 35 | 179 | DQ19 | VDD | 73 | 217 | VDD |
| DQ28 | 36 | 180 | VSS | CK0_t | 74 | 218 | CK1_t |
| VSS | 37 | 181 | DQ29 | CK0_c | 75 | 219 | CK1_c |
| DQ24 | 38 | 182 | VSS | VDD | 76 | 220 | VDD |
| | | | | VTT | 77 | 221 | VTT |

Table 4: NVDIMM Pin Assignments (continued)

| Front Side Pin Label | Pin | Pin | Back Side Pin Label | Front Side Pin Label | Pin | Pin | Back Side Pin Label |
|----------------------------------|-----|-----|---------------------|----------------------------------|-----|-----|---------------------|
| | KEY | | | | | | |
| EVENT_n | 78 | 222 | PARITY | TDQS14_c, DQS14_c, NC | 111 | 255 | DQS5_c |
| A0 | 79 | 223 | VDD | VSS | 112 | 256 | DQS5_t |
| VDD | 80 | 224 | BA1 | DQ46 | 113 | 257 | VSS |
| BA0 | 81 | 225 | A10/AP | VSS | 114 | 258 | DQ47 |
| RAS_n/A16 | 82 | 226 | VDD | DQ42 | 115 | 259 | VSS |
| VDD | 83 | 227 | RFU | VSS | 116 | 260 | DQ43 |
| CS0_n | 84 | 228 | WE_n/A14 | DQ52 | 117 | 261 | VSS |
| VDD | 85 | 229 | VDD | VSS | 118 | 262 | DQ53 |
| CAS_n/A15 | 86 | 230 | SAVE_n | DQ48 | 119 | 263 | VSS |
| ODT0 | 87 | 231 | VDD | VSS | 120 | 264 | DQ49 |
| VDD | 88 | 232 | A13 | TDQS15_t, DQS15_t, DM6_n, DBI6_n | 121 | 265 | VSS |
| CS1_n, NC | 89 | 233 | VDD | TDQS15_c, DQS15_c, NC | 122 | 266 | DQS6_c |
| VDD | 90 | 234 | NC, A17 | VSS | 123 | 267 | DQS6_t |
| ODT1, NC | 91 | 235 | NC, C2 | DQ54 | 124 | 268 | VSS |
| VDD | 92 | 236 | VDD | VSS | 125 | 269 | DQ55 |
| C0, CS2_n, NC | 93 | 237 | NC, CS3_n, C1 | DQ50 | 126 | 270 | VSS |
| VSS | 94 | 238 | SA2 | VSS | 127 | 271 | DQ51 |
| DQ36 | 95 | 239 | VSS | DQ60 | 128 | 272 | VSS |
| VSS | 96 | 240 | DQ37 | VSS | 129 | 273 | DQ61 |
| DQ32 | 97 | 241 | VSS | DQ56 | 130 | 274 | VSS |
| VSS | 98 | 242 | DQ33 | VSS | 131 | 275 | DQ57 |
| TDQS13_t, DQS13_t, DM4_n, DBI4_n | 99 | 243 | VSS | TDQS16_t, DQS16_t, DM7_n, DBI7_n | 132 | 276 | VSS |
| TDQS13_c, DQS13_c, NC | 100 | 244 | DQS4_c | TDQS16_c, DQS16_c, NC | 133 | 277 | DQS7_c |
| VSS | 101 | 245 | DQS4_t | VSS | 134 | 278 | DQS7_t |
| DQ38 | 102 | 246 | VSS | DQ62 | 135 | 279 | VSS |
| VSS | 103 | 247 | DQ39 | VSS | 136 | 280 | DQ63 |
| DQ34 | 104 | 248 | VSS | DQ58 | 137 | 281 | VSS |
| VSS | 105 | 249 | DQ35 | VSS | 138 | 282 | DQ59 |
| DQ44 | 106 | 250 | VSS | SA0 | 139 | 283 | VSS |
| VSS | 107 | 251 | DQ45 | SA1 | 140 | 284 | VDDSPD |
| DQ40 | 108 | 252 | VSS | SCL | 141 | 285 | SDA |
| VSS | 109 | 253 | DQ41 | VPP | 142 | 286 | VPP |
| TDQS14_t, DQS14_t, DM5_n, DBI5_n | 110 | 254 | VSS | VPP | 143 | 287 | VPP |
| | | | | RFU | 144 | 288 | VPP |

Table 5: NVDIMM Pin Descriptions

| Signal Name | Signal Type | Signal Description |
|----------------|-------------|---|
| Ax | Input | Address inputs: Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. |
| A10/AP | Input | Auto precharge: A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation (HIGH = Auto precharge; LOW = No auto precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses. |
| A12/BC_n | Input | Burst chop: 12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = No burst chop; LOW = Burst-chopped). See the Command Truth Table in DDR4 component data sheet for more information. |
| ACT_n | Input | Command input: ACT_n defines the activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as row address A16, A15, and A14. See the Command Truth Table in DDR4 component datasheet for more information. |
| BAx | Input | Bank address inputs: Define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. |
| BGx | Input | Bank group address inputs: Define which bank group a REFRESH, ACTIVATE, READ,WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16 based SDRAMs only have BG0. |
| C0 C1 C2 | Input | Stack address inputs: These inputs are used only when devices are stacked, that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP pack-age, which use CS1_n, CKE1, and ODT1 to control the second die. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave)-type configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code. |
| CKx_t CKx_c | Input | Clock: Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. |

Table 5: NVDIMM Pin Descriptions (Continued)

| Signal Name | Signal Type | Signal Description |
|------------------------------------|-------------|--|
| CKEx | Input | Clock enable: CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGEPOWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREFCA has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be held HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh. |
| CSx_n | Input | Chip select: All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code. |
| ODTx | Input | On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (RTT) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, RTT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed |
| PARITY | Input | Parity for command and address: This function can be enabled or disabled via the mode register. When enabled in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time with command and address with CS_n LOW. |
| RAS_n/A16 CAS_n/A15 WE_n/A14 | Input | Command inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered. Those pins have multifunction. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in the command truth table. |
| RESET_n | Input | Active LOW asynchronous reset: Reset is active when RESET_n is LOW; inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. |
| SAX | Input | Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus. |
| SCL | Input | Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus. |
| SDA | I/O | Serial Presence Detect bus bidirectional data: SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM/AGIGARAM SCU on the module on the SM bus. |

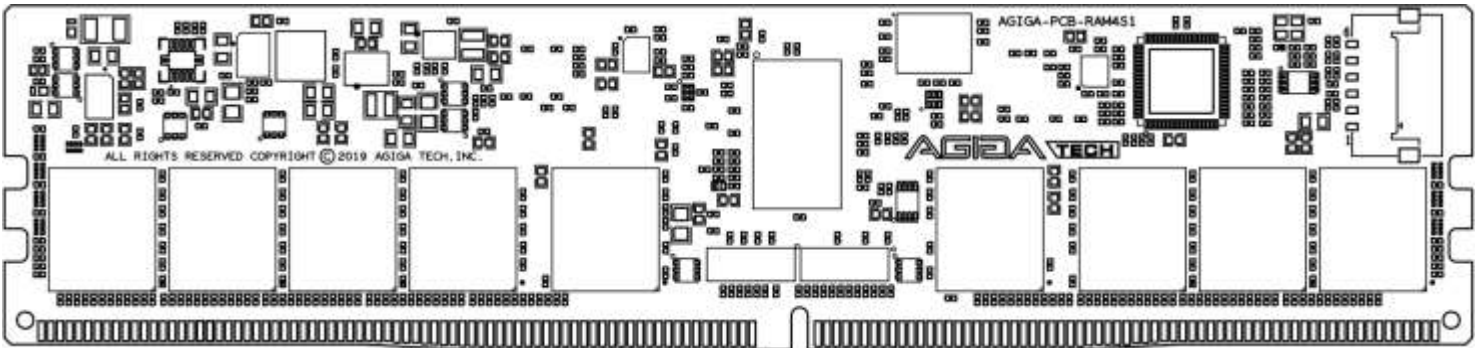
Table 5: NVDIMM Pin Descriptions (Continued)

| Signal Name | Signal Type | Signal Description |
|---|-------------|---|
| DQx, CBx | I/O | Data input/output and Check Bit input/output: Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, then CRC code is added at the end of the data burst. Either one or all of DQ0, DQ1, DQ2, or DQ3 is/are used for monitoring of internal VREF level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled. |
| DM_n/DBI_n /TDQS_t(DMU_n,DBIU_n),(DML_n/DBIU_n) | Input | Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported in x4 configurations. The UDM_n and LDM_n pins are used in the x16 configuration, UDM_n is associated with DQ[15:8]; LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See Data Mask (DM). |
| DQS_tDQS_cDQSU_tDQSU_cDQSL_tDQSL_c | I/O | Data strobe: Output with read data, input with write data. Edge-aligned with read data, centered-aligned with WRITE data. For x16 configurations, DQSL corresponds to the data on DQ[7:0]; DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0] respectively. DDR4 SDRAM support a differential data strobe only and do not support a single-ended data strobe. |
| ALERT_n | Output | Alert output: Possesses multifunction such as CRC error flag and command and address parity error flag as output signal. If there is a CRC error, then ALERT_n goes LOW for the period time interval and returns HIGH. If there is error in command address parity check, then ALERT_n goes LOW until on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Using this signal or not is dependent on the system. If not connected as signal, ALERT_n pin must be connected to VDD on DIMM. |
| EVENT_n | Output | Temperature event: The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors. |
| TDQS_tTDQS_c(x8 DRAM based RDIMM only) | Output | Termination data strobe: TDQS_t and TDQS_c are not valid for UDIMMs. When enabled via the mode register, the SDRAM enable the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For further information about TDQS, refer to DDR4 DRAM data sheet. |

Table 5: NVDIMM Pin Descriptions (Continued)

| Signal Name | Signal Type | Signal Description |
|--------------------|---------------------|---|
| V _{DD} | Supply | Power supply: 1.2V ±0.060V |
| V _{DDQ} | Supply | DQ power supply: 1.2V ±0.060V |
| V _{PP} | Supply | DRAM activating power supply: 2.5V -0.125V / +0.250V |
| V _{REFCA} | Supply | Reference voltage for control, command, and address pins. |
| V _{SS} | Supply | Ground. |
| V _{SSQ} | Supply | DQ ground. |
| ZQ | Reference | Reference ball for ZQ calibration: This ball is tied to an external 240Ω resistor(RZQ), which is tied to VSSQ. |
| RFU | - | Reserved for future use. |
| NC | - | No connect: No internal electrical connection is present. |
| NF | - | No function: Internal connection may be present but has no function. |
| SAVE_n | I/O (open drain) | SAVE_n: Active Low, open drain input that commands the AGIGARAM MCU to switch its internal muxes and copy the data in the SDRAM to internal NAND Flash. The SDRAM must be placed in Self-Refresh before asserting this pin to ensure that the no data is lost during this operation. |
| 12V | Supply | Module Power: The 12 Volt power source is optionally available for modules which support technologies other than homogeneously populated DRAM modules (i.e. not for UDIMMs, RDIMMs, and LRDIMMs). Any module which uses 12V must be enduring of power sequence(s) which do not support 12 Volts.12V is expected to remain valid during reduced power modes. The specific load requirements during those modes is product specific. |

Front View



Back View

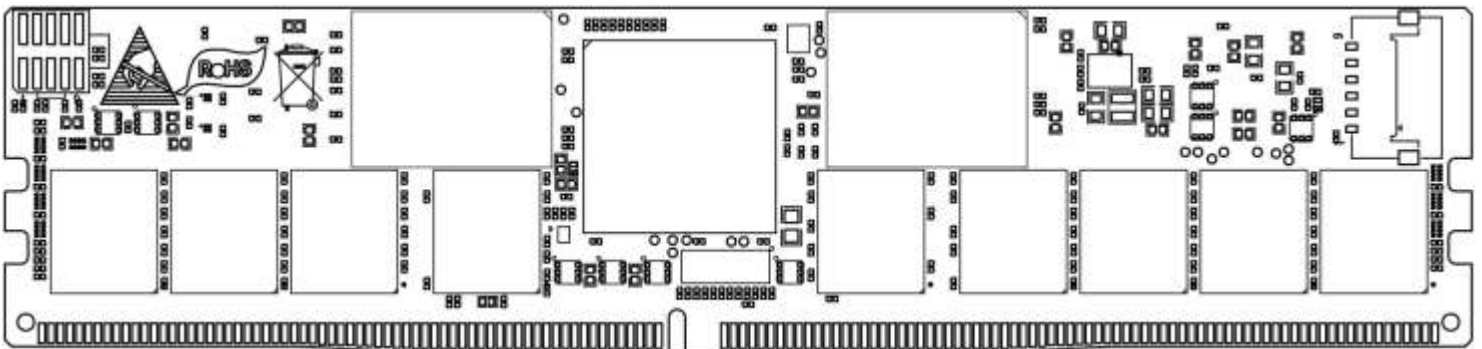


Figure 3: Connector Locations

Table 6: 6-pin Interface Connectors; Pinout and Description

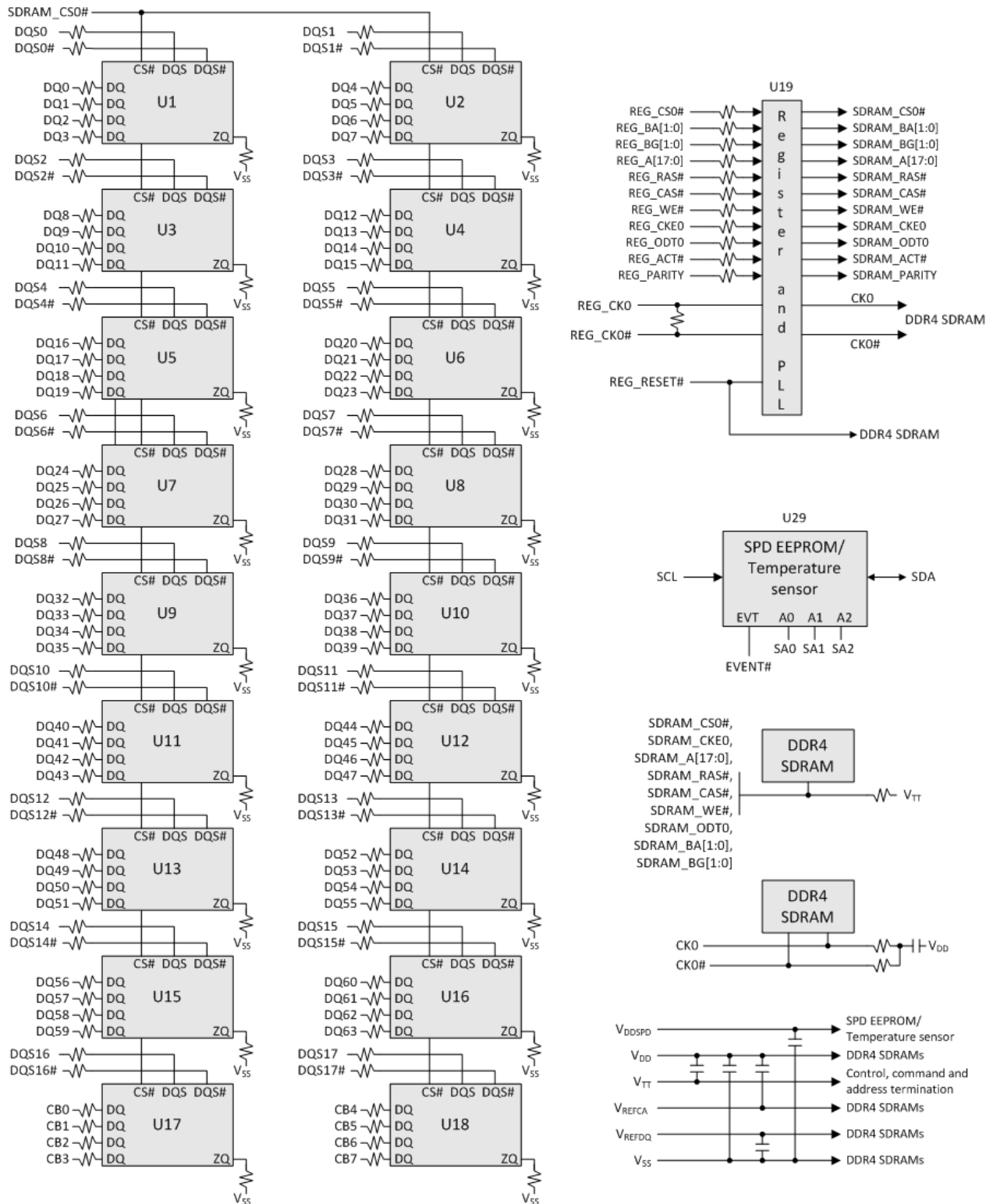
| PowerGEM Interface Connector | | | |
|------------------------------|-----------------|-------------|---|
| Pin | Signal Name | Signal Type | Description |
| 1 | PGM_SCL | Output | I ² C/SMB clock for PGEM slave unit |
| 2 | PGM_SDA | I/O | I ² C/SMB data for PGEM slave unit |
| 3 | Present | Input | The AGIGARAM can read this signal to determine if the PowerGEM is present; Reading a low voltage level, means PowerGEM is connected, and reading a high voltage level means PowerGEM is not connected. |
| 4 | GTG | Input | Active High signal indicating that PowerGEM is operational, fully charged and ready to supply power to NVDIMM for a Save operation during a Power failure. |
| 5 | V _{ss} | Supply | Ground |
| 6 | VBUS | Supply | This is a multifunction pin that provides 12V power from the host to the PowerGEM during normal operation for charging, and provides capacitor output voltage from the PowerGEM to the NVDIMM for a Save operation when there is a power loss scenario. |

6 DQ Map

Table 7: Component-to-Module DQ Map

| Component Reference Number | Component DQ | Module DQ | Module Pin Number | Component Reference Number | Component DQ | Module DQ | Module Pin Number |
|----------------------------|--------------|-----------|-------------------|----------------------------|--------------|-----------|-------------------|
| U1 | 0 | 0 | 5 | U9 | 0 | 32 | 97 |
| | 2 | 1 | 150 | | 2 | 33 | 242 |
| | 3 | 2 | 12 | | 3 | 34 | 104 |
| | 1 | 3 | 157 | | 1 | 35 | 249 |
| U2 | 3 | 4 | 3 | U10 | 3 | 36 | 95 |
| | 1 | 5 | 148 | | 1 | 37 | 240 |
| | 2 | 6 | 10 | | 2 | 38 | 102 |
| | 0 | 7 | 155 | | 0 | 39 | 247 |
| U3 | 0 | 8 | 16 | U11 | 0 | 40 | 108 |
| | 2 | 9 | 161 | | 2 | 41 | 253 |
| | 3 | 10 | 23 | | 3 | 42 | 115 |
| | 1 | 11 | 168 | | 1 | 43 | 260 |
| U4 | 3 | 12 | 14 | U12 | 3 | 44 | 106 |
| | 1 | 13 | 159 | | 1 | 45 | 251 |
| | 2 | 14 | 21 | | 2 | 46 | 113 |
| | 0 | 15 | 166 | | 0 | 47 | 258 |
| U5 | 0 | 16 | 27 | U13 | 0 | 48 | 119 |
| | 2 | 17 | 172 | | 2 | 49 | 264 |
| | 3 | 18 | 34 | | 3 | 50 | 126 |
| | 1 | 19 | 179 | | 1 | 51 | 271 |
| U6 | 3 | 20 | 25 | U14 | 3 | 52 | 117 |
| | 1 | 21 | 170 | | 1 | 53 | 262 |
| | 2 | 22 | 32 | | 2 | 54 | 124 |
| | 0 | 23 | 177 | | 0 | 55 | 269 |
| U7 | 0 | 24 | 38 | U15 | 0 | 56 | 130 |
| | 2 | 25 | 183 | | 2 | 57 | 275 |
| | 3 | 26 | 45 | | 3 | 58 | 137 |
| | 1 | 27 | 190 | | 1 | 59 | 282 |
| U8 | 3 | 28 | 36 | U16 | 3 | 60 | 128 |
| | 1 | 29 | 181 | | 1 | 61 | 273 |
| | 2 | 30 | 43 | | 2 | 62 | 135 |
| | 0 | 31 | 188 | | 0 | 63 | 280 |
| U17 | 0 | CB0 | 49 | U18 | 3 | CB4 | 47 |
| | 2 | CB1 | 194 | | 1 | CB5 | 192 |
| | 3 | CB2 | 56 | | 2 | CB6 | 54 |
| | 1 | CB3 | 201 | | 0 | CB7 | 199 |

7 Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω 1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Figure 4: Functional Block Diagram

8 General DDR4 RDIMM Functional Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. DDR4 SDRAM modules utilizing 4-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing a total of 16 banks. Sixteen-bit-wide DDR4 SDRAM has 2 internal bank groups consisting of 4 memory banks each, providing a total of 8 banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single $8n$ -bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

8.1 Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signal can be easily accounted for by using the write-leveling feature of DDR4.

8.2 Registering Clock Driver Operation

Registered DDR4 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC DDR4 Register Specification.

The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and re-drives the differential clock signals (CK, CK#) to the DDR4 SDRAM devices. The registering clock driver(s) reduces clock, control, command, and address signal loading by isolating DRAM from the system controller.

8.3 Parity Operations

The registering clock driver includes a parity-checking function that can be enabled or disabled in control word RCOE. When parity checking is enabled, the registering clock driver forwards sampled commands to the SDRAM only when no parity error has occurred. If the parity error function has been disabled, the registering clock driver forwards sampled commands to the DRAM regardless of whether a parity error has occurred. Parity is also checked during control word WRITE operations unless parity checking is disabled.

The registering clock driver receives a parity bit at the DPAR input from the memory controller and compares it with the data received on the qualified CA inputs and indicates on its open-drain ALERT_n pin whether a parity error has occurred. Valid parity is defined as an even number of 1s across the address and command inputs qualified by at least one of the DCS[n:0] signals being LOW.

9 Temperature Sensor with Serial Presence-Detect EEPROM

9.1 Thermal Sensor Operations

The temperature from the integrated thermal sensor is monitored and converted to a digital word via the I²C/SM Bus (SMB). System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1 "Definition of the TSE2004av, Serial Presence Detect with Temperature Sensor."

9.2 Serial Presence-Detect EEPROM Operation

DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte EEPROM. The first 384 bytes are programmed to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR4 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM's SCL(clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection. Agiga implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0–383) from being inadvertently programmed or corrupted. The upper 128 bytes will remain available and unprotected.

10 Timing Parameters

There are several system level timing parameters that are specific to the operation of a NVDIMM. This table outlines these parameters.

Table 8: Timing Parameters

| Parameter/Condition | Symbol | Typical | Max | Units | Notes | |
|--|-------------------|---------|-----|---------|-------|------|
| Time for AGIGARAM controller to be able to respond to SM bus commands from a powerup condition | t_{HW_RDY} | 9 | 80 | s | 1 | |
| Time for AGIGARAM controller to copy DRAM contents to NAND flash | t_{SAVE} | 16GB | 34 | 38 | s | 2, 3 |
| | | 32GB | 34 | 38 | | |
| Time for AGIGARAM controller to copy an image in NAND flash to DRAM | $t_{RESTORE}$ | 16GB | 38 | 65 | s | 4 |
| | | 32GB | 38 | 65 | | |
| Time from Issuing a Release NAND Flash command to reporting sufficient NAND Flash available for a save | t_{R_NF} | 4 | 8 | s | | |
| Time it takes for AGIGARAM controller to switch the muxes once a Save trigger is asserted. During this time the host must maintain VDD within the operating range and keep the DIMM in self refresh or data could be potentially lost. | t_{MUX_SWITCH} | 3 | 5 | μs | | |

- Notes:
- 1) Max time will be reached when the NVDIMM is reset following a firmware update and the system finds an issue with the firmware image that causes the system to reload the default image.
 - 2) If the AgigA NVDIMM encounters errors during the SAVE, it will continue to attempt to save until it either runs out of power or a command is sent to the NVDIMM to cancel the SAVE operation.
 - 3) Assumes 1x NAND placement for 16GB and 2x1TB NAND for 32GB, Komodo1 supports up to 2x placements
 - 4) Max restore time based on a 10,000 ECC correction limit on the NAND flash.

11 Design Considerations

11.1 Simulations

AgigA Tech memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. AgigA Tech encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

11.2 Power

Operating voltages are specified at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

12 Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device’s data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 9: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Notes |
|------------------------------------|---|------|------|-------|-------|
| V _{DD} | V _{DD} supply voltage relative to V _{SS} | -0.4 | +1.5 | V | 1 |
| V _{DDQ} | V _{DDQ} supply voltage relative to V _{SS} | -0.4 | +1.5 | V | 1 |
| V _{PP} | Voltage on V _{PP} pin relative to V _{SS} | -0.4 | 3.0 | V | 2 |
| V _{IN} , V _{OUT} | Voltage on any pin relative to V _{SS} | -0.4 | +1.5 | V | |
| 12V | Module Voltage | -0.4 | 13.8 | V | |
| T _{STORAGE} | Storage Temperature | -50 | +100 | °C | |

Notes: 1)V_{DDQ} balls on DRAM are tied to V_{DD}.
 2)V_{PP} must be greater than or equal to V_{DD} at all times.

For the purpose of this document, the I_{DD} supply current will be defined in two groups. The sum of these groups represents the overall current consumption for the part.

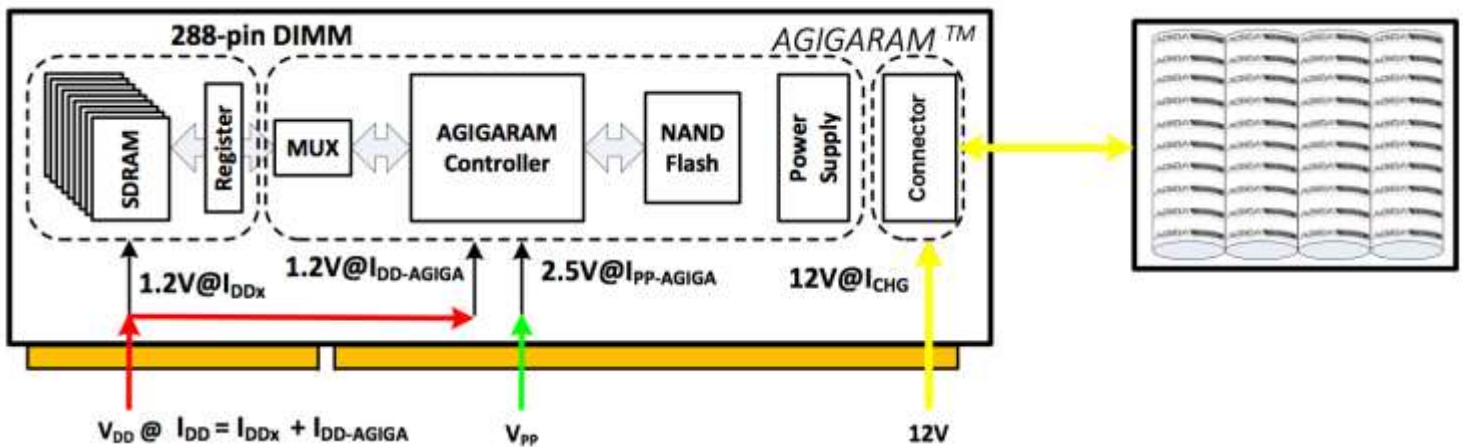


Figure 5: System Supply Current Diagram

Table 10: Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units | Notes | |
|------------------------|--|--------------------------------|-----------------------|--------------------------------|-------|--------|----|
| V _{DD} | V _{DD} supply voltage | 1.14 | 1.20 | 1.26 | V | 1 | |
| V _{PP} | DRAM Activating Power Supply | 2.375 | 2.5 | 2.750 | V | 2 | |
| 12V | Host Power for NVDIMM(Operation) | 10.2 | 12 | 13.8 | V | | |
| | Save Power for NVDIMM (Power off) | 4 | | 13.8 | V | | |
| I _{DD} | I _{DD} supply current = I _{DDx} + I _{DD-AGIGA} | | | | | | |
| I _{DDx} | I _{DDx} current from input supply voltage during By-Pass or host memory access mode. Details for specific DRAM operating modes can be found in the I _{DDx} tables. | 16GB | 0.054 | - | 3.942 | A | 3 |
| | | 32GB | 0.036 | | 3.546 | A | 3 |
| I _{DD-AGIGA} | AGIGARAM controller current from input supply voltage during normal operation | - | 50 | 100 | mA | | |
| I _{CHG} | I _{DD-CHG} current from input supply voltage during ultracapacitor charging | 0 | - | 1 | A | 4 | |
| V _{REFCA(DC)} | Input reference voltage command/address bus | 0.49 x V _{DD} | 0.5 x V _{DD} | 0.51 x V _{DD} | V | 5 | |
| V _{TT} | Termination reference voltage (DC)-command/address bus | 0.49 x V _{DD} - 20 mV | 0.5 x V _{DD} | 0.51 x V _{DD} + 20 mV | V | 6 | |
| I _{IN} | Input leakage current; Any input excluding ZQ; 0V < V _{IN} < 1.1V | -2 | - | 2 | μA | 7 | |
| I _{ZQ} | Input leakage current; ZQ | -3 | - | +3 | μA | 8,9 | |
| I _{I/O} | DQ leakage; 0V < V _{IN} < V _{DD} | -4 | - | +4 | μA | 9 | |
| I _{OZpd} | Output leakage current; V _{OUT} = V _{DD} ; DQ are disabled | - | - | 5 | μA | | |
| I _{OZpu} | Output leakage current; V _{OUT} = V _{SS} ; DQ and ODT are disabled; ODT is disabled with ODT input HIGH | - | - | 50 | μA | | |
| I _{VREFCA} | V _{REFCA} leakage; V _{REFCA} = V _{DD} /2 (After DRAM is initialized) | -2 | 0 | +2 | μA | 9 | |
| T _{OPER} | Normal operating temperature range | 0 | - | 55 | °C | 10, 11 | |
| J _{SAVE} | Required Joules to perform a SAVE operation | 16GB | - | - | 140 | J | 12 |
| | | 32GB | | | 210 | J | 12 |

- Notes:
- 1) V_{DDQ} balls on DRAM are tied to V_{DD}.
 - 2) V_{PP} must be greater than or equal to V_{DD} at all times.
 - 3) Numbers measured using 3200 speed modules.
 - 4) Some PowerGEMs utilize external charging, so this number could be zero. See PowerGEM datasheet for details.
 - 5) V_{REFCA} MUST not be greater than 0.6 x V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
 - 6) V_{TT} termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins and reduce timing margins.
 - 7) Command and address inputs are terminated to V_{DD}/2 in the registering clock driver. Input current is dependent on termination resistance set in the registering clock driver.
 - 8) Tied to ground. Not connected to edge connector.
 - 9) Multiply by number of DRAM die on module.

10) DRAM T_{case} is rated up to 95°C

11) For additional information, refer to tech note TN-00-08: "Thermal Applications" available on Micron's web site.

12) Used by host to determine energy requirement for host managed energy source.

13 IDDx Specifications

Values are for a 16GB NVDIMM are computed from values specified in the 8Gb (2Gig x 4) component data sheet.

Table 11: DDR4 IDDx Specification and Conditions

| Parameter | Symbol | 2933 | 3200 | Units |
|---|--------------------|-------|-------|-------|
| One bank ACTIVATE-PRECHARGE current | I _{DD0} | 738 | 774 | mA |
| One bank ACTIVATE-PRECHARGE, word line boost, IPP current | I _{PP0} | 54 | 54 | mA |
| One bank ACTIVATE-READ-PRECHARGE current | I _{DD1} | 954 | 990 | mA |
| Precharge standby current | I _{DD2N} | 540 | 558 | mA |
| Precharge standby ODT current | I _{DD2NT} | 720 | 756 | mA |
| Precharge power-down current | I _{DD2P} | 396 | 396 | mA |
| Precharge quiet standby current | I _{DD2Q} | 468 | 468 | mA |
| Active standby current | I _{DD3N} | 720 | 756 | mA |
| Active standby IPP current | I _{PP3N} | 54 | 54 | mA |
| Active power-down current | I _{DD3P} | 558 | 576 | mA |
| Burst read current | I _{DD4R} | 2430 | 2610 | mA |
| Burst write current | I _{DD4W} | 2106 | 2268 | mA |
| Distributed refresh current (1X REF) | I _{DD5R} | 828 | 846 | mA |
| Distributed refresh IPP current (1X REF) | I _{PP5R} | 90 | 90 | mA |
| IDD6N: Self refresh current; -40–85°C | I _{DD6N} | 576 | 576 | mA |
| Self refresh current; -40–95°C | I _{DD6E} | 990 | 990 | mA |
| Self refresh current; -40–45°C | I _{DD6R} | 360 | 360 | mA |
| Auto self refresh current (25°C) | I _{DD6A} | 147.6 | 147.6 | mA |
| Auto self refresh current (45°C) | I _{DD6A} | 360 | 360 | mA |
| Auto self refresh current (75°C) | I _{DD6A} | 540 | 540 | mA |
| Auto self refresh current (95°C) | I _{DD6A} | 990 | 990 | mA |
| Auto self refresh IPP current; -40–95°C | I _{PP6X} | 90 | 90 | mA |
| Bank interleave read current | I _{DD7} | 3690 | 3942 | mA |
| Bank interleave read IPP current | I _{PP7} | 198 | 198 | mA |
| Maximum power-down current | I _{DD8} | 324 | 324 | mA |

Values are for a 32GB NVDIMM are computed from values specified in the 16Gb (4Gig x 4) component data sheet.

Table 12: DDR4 IDDx Specification and Conditions

| Parameter | Symbol | 2933 | 3200 | Units |
|---|--------------------|------|------|-------|
| One bank ACTIVATE-PRECHARGE current | I _{DD0} | 972 | 990 | mA |
| One bank ACTIVATE-PRECHARGE, word line boost, IPP current | I _{PP0} | 54 | 54 | mA |
| One bank ACTIVATE-READ-PRECHARGE current | I _{DD1} | 1170 | 1188 | mA |
| Precharge standby current | I _{DD2N} | 792 | 810 | mA |
| Precharge standby ODT current | I _{DD2NT} | 900 | 918 | mA |
| Precharge power-down current | I _{DD2P} | 684 | 684 | mA |
| Precharge quiet standby current | I _{DD2Q} | 756 | 756 | mA |
| Active standby current | I _{DD3N} | 1062 | 1080 | mA |
| Active standby IPP current | I _{PP3N} | 36 | 36 | mA |
| Active power-down current | I _{DD3P} | 846 | 864 | mA |
| Burst read current | I _{DD4R} | 2142 | 2286 | mA |
| Burst write current | I _{DD4W} | 1818 | 1890 | mA |
| Distributed refresh current (1X REF) | I _{DD5R} | 1224 | 1224 | mA |
| Distributed refresh IPP current (1X REF) | I _{PP5R} | 72 | 72 | mA |
| IDD6N: Self refresh current; -40–85°C | I _{DD6N} | 954 | 954 | mA |
| Self refresh current; -40–95°C | I _{DD6E} | 2034 | 2034 | mA |
| Self refresh current; -40–45°C | I _{DD6R} | 360 | 360 | mA |
| Auto self refresh current (25°C) | I _{DD6A} | 198 | 198 | mA |
| Auto self refresh current (45°C) | I _{DD6A} | 360 | 360 | mA |
| Auto self refresh current (75°C) | I _{DD6A} | 918 | 918 | mA |
| Auto self refresh current (95°C) | I _{DD6A} | 2034 | 2034 | mA |
| Auto self refresh IPP current; -40–95°C | I _{PP6X} | 108 | 108 | mA |
| Bank interleave read current | I _{DD7} | 3510 | 3546 | mA |
| Bank interleave read IPP current | I _{PP7} | 162 | 162 | mA |
| Maximum power-down current | I _{DD8} | 648 | 648 | mA |

14 Registering Clock Driver Specifications

DDR4 RCD01 devices or equivalent

Table 13: Registering Clock Driver Electrical Characteristics

| Parameter | Symbol | Pins | Min | Nom | Max | Units |
|--|---------------------------|----------------------------|---------------------------------|----------------------|---------------------------------|---------|
| DC supply voltage | V_{DD} | – | 1.14 | 1.2 | 1.26 | V |
| DC reference voltage | V_{REF} | V_{REFCA} | $0.49 \times V_{DD}$ | $0.5 \times V_{DD}$ | $0.51 \times V_{DD}$ | V |
| DC termination voltage | V_{TT} | – | $V_{REF} - 40mV$ | V_{REF} | $V_{REF} + 40mV$ | V |
| High-level input voltage | $V_{IH, CMOS}$ | DRST_n | $0.65 \times V_{DD}$ | – | V_{DD} | V |
| Low-level input voltage | $V_{IL, CMOS}$ | DRST_n | 0 | – | $0.35 \times V_{DD}$ | V |
| DRST_n pulse width | $t_{INIT_Power_stable}$ | – | 1.0 | – | – | μs |
| AC high-level output voltage | $V_{OH(AC)}$ | All outputs except ALERT_n | $V_{TT} + (0.15 \times V_{DD})$ | – | – | V |
| AC low-level output voltage | $V_{OL(AC)}$ | All outputs except ALERT_n | – | – | $V_{TT} + (0.15 \times V_{DD})$ | V |
| AC differential out- put high measurement level (for output slew rate) | $V_{OHdiff(AC)}$ | Yn_t - Yn_c, BCK_t - BCK_c | – | $+0.3 \times V_{DD}$ | – | mV |
| AC differential out- put low measurement level (for output slew rate) | $V_{OLDiff(AC)}$ | Yn_t - Yn_c, BCK_t - BCK_c | – | $-0.3 \times V_{DD}$ | – | mV |

Note: Timing and switching specifications for the register listed are critical for proper operation of the DDR4 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Please refer to JEDEC RCD01 specification for complete operating electrical characteristics. RCD parametric values are specified for device default control word settings, unless otherwise stated. The RCOA control word setting does not affect parametric values.

15 LED Indicators

AGIGARAM contains three LEDs on the back of the PCB for providing status information:

Table 14: LED Functions

| LED | State | Function |
|--------------------------|--|---|
| Blue Save/Restore LED | Fast Blink (On for 100 ms/Off for 200 ms) | When a SAVE_n or a RESTORE is in progress |
| | Slow Blink (heartbeat, every 15 seconds) | Normal Operation |
| Amber User LED | ON/OFF | The state of this LED is user configurable, see the firmware specification for details on turning this LED on or off. NOTE: The LED may blink briefly in Amber when the NVDIMM first powers on. This is normal and does not indicate an error. |
| Green Power LED | ON | When AGIGARAM Controller power is present |
| | OFF | When AGIGARAM Controller power is NOT present |

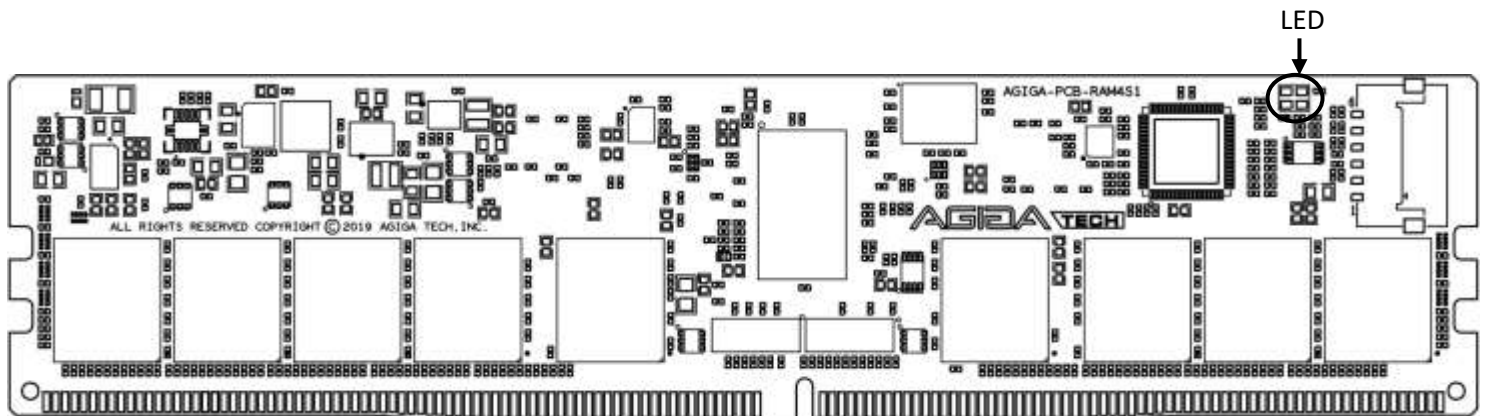


Figure 6: AGIGARAM LED Locations

16 Part Numbers

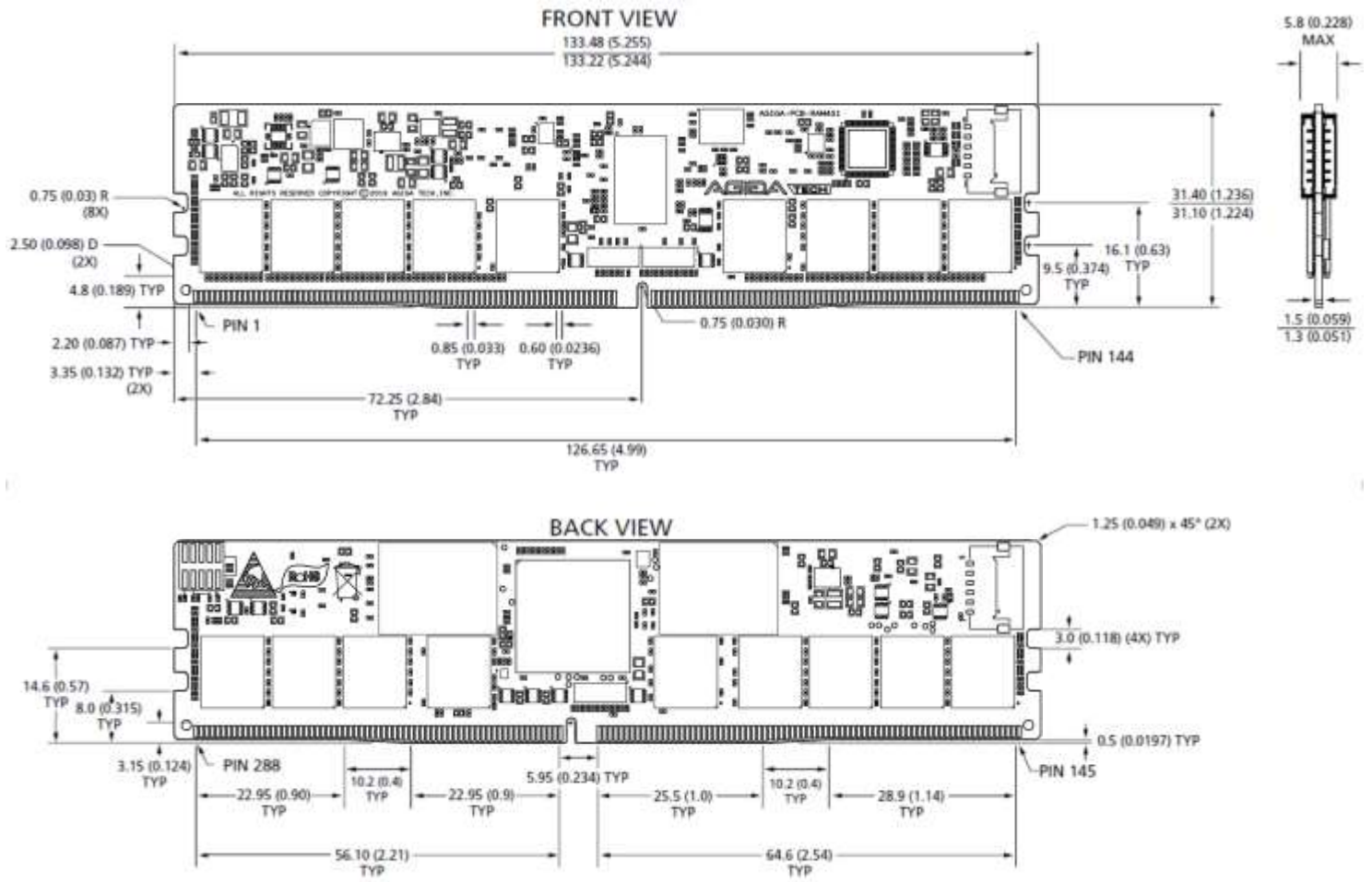
Table 15: Komodo1 Part Numbers

| PART NUMBER | DESCRIPTION | COMMENTS | NOTES |
|------------------|---|--|-------|
| AGIGA8811-016ACA | 16GB DDR4-3200 NVDIMM-N 1.2V, SRx4, x72 DRAM | JEDEC FW support, 2K pull-up on SAVE_N | 1, 2 |
| AGIGA8811-016ACB | 16GB DDR4-3200 NVDIMM-N 1.2V, SRx4, x72 DRAM | JEDEC FW support, NO pull-up on SAVE_N | 1, 2 |
| AGIGA8811-032ACA | 32GB DDR4-3200 NVDIMM-N 1.2V, SRx4, x72 DRAM | JEDEC FW support, 2K pull-up on SAVE_N | 1, 2 |
| AGIGA8811-032ACB | 32GB DDR4-3200 NVDIMM-N 1.2V, SRx4, x72 DRAM | JEDEC FW support, NO pull-up on SAVE_N | 1, 2 |

Note 1: Each NVDIMM module must be paired with an appropriate PowerGEM module for proper operation (or must be operated in Central Power Mode, see FW spec for more details). Please contact Agiga Tech for available PowerGEM options.

Note 2: Some older servers were designed without any pullup resistor on the SAVE_n signal. For these systems, you must use an NVDIMM with the pull-up resistor or the SAVE_n signal will be a floating input to the NVDIMM controller. In some cases, this could be a leakage path for the NVDIMM PowerGEM energy to back power the host system when the host system has lost power and the NVDIMM is powered via the PowerGEM and performing a Save operation. New systems have now added a pull-up resistor on the server motherboard and an NVDIMM without the pull-up resistor(ACB versions) should be used for this configuration.

17 Module Dimensions



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only.

Figure 7: AGIGARAM Mechanical Dimensions